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Application No. 00/845584	Prepared by	M RUSTIA	Tracking Number	0603538
Examiner-GAU MYERS - 2/12	Date	10-01-04	Week Date	08-30-04
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a. Serial No.	f. Foreign Priority	k. Print Claim(s)	(p.)PTO-1449		
b. Applicant(s)	g. Disclaimer	I. Print Fig.	q. PTOL-85b		
c. Continuing Data	h. Microfiche Appendix	m. Searched Column	r. Abstract		
d. PCT	i. Title	n. PTO-270/328	s. Sheets/Figs		
e. Domestic Priority	j. Claims Allowed	o. PTO-892	t. Other		

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Application Number: 09/845,504

Filing Date: 04-30-2001

First Named Inventor: Kenneth Kotlowski

Group Art Unit: 2112

Examiner Name: Paul R. Myers Attorney Docket Number: 1458-P04919

U.S. PATENT DOCUMENTS

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Examiner Initials *	Cite No.1	U.S. Patent Document Number Kind Code 2 (If innown)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Refevent Passages or Relevent Figures Appear	
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	A11	JP	410285011	A	Aihara	10-23-1998	Abstract only	X
	A12	DE	19949144	C1	Goetz	01-01-2001	Abstract only	X
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	A15	John P. Uyemura, "CMOS Logic Circuit Design," Kluwer Academic Publishers, Boston, MA; ISBN 0-7923-8452-0, pp. 144 & 145	2001
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ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18
Stylesheet Version v18.0

Title of Invention

SPLIT TRANSACTIONAL UNIDIRECTIONAL BUS ARCHITECTURE AND METHOD OF OPERATION

Application Number:

09/845504

Confirmation Number:

2092

First Named Applicant:

Kenneth Kotlowski

Attorney Docket Number: 1458-P04919

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Art Unit:

2112

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Examiner: Search string: Paul R. Myers (4969120 or 5007011 or 5412786 or 5539739

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or 5581729 or 5623644 or 5634043 or 5717343 or 5740346 or 5859550 or 5933610 or 5991824 or 5248906 or 5528172 or 5996037 or 6145039 or 6185629 or 6205524 or 6256693 or 6292025 or 6335935 or 6415424 or 6504817 or 6578098

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init	Cite.No.	Pub. No.	Date	Applicant	Kind	Class	Subclass
	1	20020120878	2002-08-29	Lapidus	A1		
	2	20020110120	2002-08-15	Hagglund et al.	A1		

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